WHAT IS CLAIMED IS:

1. A system comprising:

a bus;

a first transmitter connected to the bus and configured to transmit a first signal over the bus in a first frequency band;

a second transmitter connected to the bus and configured to transmit a second signal over the bus in a second frequency band at the same time that the first transmitter is transmitting the first signal;

a first receiver connected to the bus and configured to receive the first signal transmitted over the bus in the first frequency band; and

a second receiver connected to the bus and configured to receive the second signal transmitted over the bus in the second frequency band,

wherein the first frequency band and the second frequency band occupy different portions of the frequency spectrum.

2. The system of claim 1 wherein the first transmitter includes a first filter having a first cutoff frequency defining at least in part the first frequency band.

3. The system of claim 1 wherein the first transmitter includes a first encoder defining at least in part the first frequency band.

4. The system of claim 3 wherein the first encoder has a defined first run length defining at least in part the first frequency band.

5. The system of claim 3 wherein the first encoder comprises a combinational logic table.

6. The system of claim 1 wherein the first transmitter and the second receiver are part of a single chip.

7. The system of claim 1 wherein the first frequency band and the second frequency band are fixed.

8. The system of claim 1 further comprising a band setting unit configured to set the first frequency band and the second frequency band in response to an input signal.

9. The system of claim 8 further comprising a user selection device configured to generate the input signal.

10. The system of claim 8 further comprising a first arbitration module and a second arbitration module configured to arbitrate between one another to generate the input signal.

11. The system of claim 1 wherein the first transmitter and the second receiver are associated with a microprocessor.

12. The system of claim 1 wherein the first transmitter and the second receiver are associated with a memory storage device.

13. The system of claim 1 wherein the first transmitter and the second receiver are associated with a chipset.

14. The system of claim 1 wherein:

the first transmitter includes a first output connected to the bus;

the second transmitter includes a second output connected to the bus;

the first receiver includes a first input connected to the bus; and

the second receiver includes a second input connected to the bus.

15. A microprocessor comprising:

a transmitter configured to transmit a first signal over a bus in a first frequency band; and

a receiver configured to receive a second signal simultaneously transmitted over the bus in a second frequency band,

wherein the first frequency band and the second frequency band occupy different portions of the frequency spectrum.

16. The microprocessor of claim 15 wherein the transmitter includes a first filter having a first cutoff frequency defining at least in part the first frequency band.

17. The microprocessor of claim 15 wherein the transmitter includes a first encoder defining at least in part the first frequency band.

18. The microprocessor of claim 15 wherein the first frequency band and the second frequency band are fixed.

19. A memory comprising:

a transmitter configured to transmit a first signal over a bus in a first frequency band; and

a receiver configured to receive a second signal simultaneously transmitted over the bus in a second frequency band,

wherein the first frequency band and the second frequency band occupy different portions of the frequency spectrum.

20. The memory of claim 19 wherein the transmitter includes a first filter having a first cutoff frequency defining at least in part the first frequency band.

21. The memory of claim 19 wherein the transmitter includes a first encoder defining at least in part the first frequency band.

22. The memory of claim 19 wherein the first frequency band and the second frequency band are fixed.

23. A chipset device comprising:

a transmitter configured to transmit a first signal over a bus in a first frequency band; and

a receiver configured to receive a second signal simultaneously transmitted over the bus in a second frequency band,

wherein the first frequency band and the second frequency band occupy different portions of the frequency spectrum.

24. The chipset device of claim 23 wherein the transmitter includes a first filter having a first cutoff frequency defining at least in part the first frequency band.

25. The chipset device of claim 23 wherein the transmitter includes a first encoder defining at least in part the first frequency band.

26. The chipset device of claim 23 wherein the first frequency band and the second frequency band are fixed.

27. A method of transmitting data within a device, comprising:

transmitting a first signal over a bus in a first frequency band;

transmitting a second signal over the bus in a second frequency band;

receiving the first signal transmitted over the bus; and

receiving the second signal transmitted over the bus, wherein:

the first frequency band and the second frequency band occupy different portions of the frequency spectrum; and

transmitting the first signal, transmitting the second signal, receiving the first signal, and receiving the second signal all occur simultaneously.

28. The method of claim 27 wherein transmitting the first signal includes encoding an output to form the first signal in the first frequency band.

29. The method of claim 28 wherein transmitting the first signal includes encoding an output to form the first signal with a defined first run length.

30. The method of claim 27 further comprising setting a spectral band of the first frequency band and the second frequency band based upon a set signal.

31. The method of claim 30 further comprising generating the set signal by arbitrating between two components on the bus.

32. The method of claim 30 further comprising generating the set signal by receiving a selection signal from a user.

33. The method of claim 27 wherein:
transmitting the first signal includes requesting memory data from a memory; and

transmitting the second signal includes returning memory data from a memory.